Docket No.: 60188-415 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Takenobu KISHIDA, et al.	:	Confirmation Number: 3663
Application No.: 10/036,388 **Patent No.: 6,770,977 B2**	:	Group Art Unit: 2814
Filed: January 07, 2002 Issued: August 3, 2004	:	Examiner: Phat X. CAO
For: SEMICONDUCTOR DEVICE INCLUDING A LAYER HAVING A B-CRYSTAL STRUCTURE (As Amended)	:	

Corrected REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 CFR 1.322

Mail Stop 4 (Certificate of Correction)
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to your Notification of Return of Papers re Request for Certificate of Correction of October 22, 2004, we are resubmitting our previously filed Request for Certificate of Correction now showing the correct patent number in the header of our Request paper so that the patent numbers on the Request and on Form 1050 agree. **The correct patent number is 6,770,977**. Copies of your Notification, as well as our previously filed Request papers are attached.

We look forward to receiving the requested Certificate of Correction.

Please charge any shortage in fees due in connection with the filing of this paper to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,
MCDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington, DC 20005-3096
202.756.8000 MEF:BD
Facsimile: 202.756.8087
Date: December ~~21~~ 23, 2004
BD

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450
www.uspto.gov

Paper No.: _____

PATENT NO.	PATENT DATE
6770,970	Jan07, 2002
PATENTEE	
Takenobu Nishida, et al.	

MAILING DATE
Certificate
OCT 22 2004
of Correction

NOTIFICATION OF RETURN OF PAPERS
RE REQUEST FOR CERTIFICATE OF CORRECTION

The request for a Certificate of Correction in the above-identified patent is returned herewith, together with the PTOL-1050 (SB/44) forms (if submitted), for the reason(s) checked below.

☐ 1. The request is unsigned. The request must be properly signed before it will be considered.

☐ 2. The request does not specifically designate the column and line numbers wherein the errors appear in the patent. A substitute request providing this information is required, for proper consideration.

☐ 3. The FORM PTOL-1050 (SB/44) submitted with your request is not suitable for printing purposes. See the instructions on the blank Form PTO-1050, enclosed.

☒ 4. The Patent No., as shown on papers attach, appears to be incorrect, because:
- ☒ a. The Patent No. on the request and on the PTO-1050 do not agree.
- ☐ b. The name of the patentee on the patented file does not agree with that shown on the enclosed papers..

☐ 5. The record reveals that there is no power of attorney to you in this case. A written power or authorization from the patentee, or assignee, if any, must be submitted, before the request may be considered.

☐ 6. The request cannot be considered, because the paper indicated below was filed on _____, AFTER payment of the issue fee: [See 37 CFR 1.313(B.].
- ☐ a. Amendment purported to be under Rule 312.
- ☐ b. Assignment.
- ☐ c. Priority papers.
- ☐ d. Other (identify) _____

☐ 7. Other: _____

☐ A. PLEASE RETURN A COPY OF THIS LETTER TOGETHER WITH THE ENCLOSED PAPERS AS CORREECTED TO ENSURE EXPEDIENT ASSOCIATION WITH THE FILE

☐ B. Enclosed are copies of PTOL-1050 for use in typing the subject matter to be printed on the Certificate. This will avoid delay in handling request (See 862 O.G.2).

Decisions and Certificate of Correction Branch

31 JAN 2005

FORM PTOL-396 (8/75)

Docket No.: 60188-415

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Takenobu KISHIDA, et al.	:	Confirmation Number: 3663
Application No.: 10/036,388	:	Group Art Unit: 2814
Patent No.: ~~6,770,970 B2~~ 6770977 B2	:	
Filed: January 07, 2002	:	Examiner: Phat X. CAO
Issued: August 3, 2004	:	

For: SEMICONDUCTOR DEVICE INCLUDING A LAYER HAVING A β-CRYSTAL STRUCTURE (As Amended)

REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 CFR 1.322

Mail Stop 4 (Certificate of Correction)
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reviewing the above-identified patent, a printing error was discovered therein requiring correction in order to conform the Official Record in the application.

The error noted is set forth on the attached copy of form PTO-1050 Rev. 2-93 in the manner required by the Commissioner's Notice.

Specifically, the title on the cover page of the printed patent, as well as at the top of Column 1, is incorrect. Please change the title from "SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME" to --**SEMICONDUCTOR DEVICE INCLUDING A LAYER HAVING A β-CRYSTAL STRUCTURE**--. The correct title can be found in Applicant's

31 JAN 2005

amendment of November 6, 2003, a copy of which is attached for your information and convenience.

The change requested herein occurred as a result of printing the Letters Patent and the Certificate should be issued without expense under Rule 322 of the Rules of Practice. Accordingly, Applicants request issuance of the Certificate of Correction.

Please charge any shortage in fees due in connection with the filing of this paper to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP

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Facsimile: 202.756.8087
Date: October 18, 2004

WDC99 992408-1.060188.0415

31 JAN 2005

Staple Here Only !

PRINTER'S TRIM LINE

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,770,977 B2

DATED : August 03, 2004

INVENTOR(S): Takenobu KISHIDA, et al.

It is certified that error appears in the above-identified patent and that said Letter Patent is hereby corrected as shown below:

On the title page of the patent, as well as at the top of Column 1, please change the title from "SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME" to --SEMICONDUCTOR DEVICE INCLUDING A LAYER HAVING A β-CRYSTAL STRUCTURE--.

31 JAN 2005

Remarks: FICE FAX

Applicant: Tetsuenobu KISHIDA, et al. Docket No. 60188-415

Title: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME Serial/Reg./Patent No. 10/036,388

Date Sent: 11/6/2003 ☒ Hand Carried ☐ Fax ☐ Electronic ☐ Cert. of Mailing ☐ Express Mail No. _____

☐ Transmittal Letter

New Patent App ☐ Utility ☐ Design ☐ Cont. ☐ CIP ☐ Div. ☐ PCT ☐ RCE ☐ Prov

☐ Other: _____

_____ pages of Specification

_____ pages of Claims

_____ pages of Abstract

_____ pages of Formal/Informal Drawings

☐ Small Entity ☐ Large Entity

☐ Declaration/Power of Attorney

☐ Recordation of Assignment/Security Agreement

☐ Information Disclosure Statement

_____ Form PTO 1449

_____ copies of cited references

☐ Preliminary Amendment

☐ Response to Missing Parts Notice

☐ Resp. to Notice to Correct App. Papers

☐ Certified Copy of Priority Doc.

☐ Claim for Convention Priority

☒ Response/Amendment to Office Action of 9/19/03

Request for ____ month Extension of Time

☐ Letter submitting ____ pages of drawings

☐ Req. for Approval of Drawing Amendments

☐ Req. for Oral Hearing

☐ Not. of Appeal ☐ Appeal Brief ☐ Reply Brief

☐ Rule 312 Amendment/Letter

☐ Req. for Acknowledgement of Cited Art

☐ Issue Fee

☐ Publication Fee

☐ Req. for Certificate of Correction

☐ Maintenance Fee for ____ years after grant

☐ Fee Address Indication Form

☐ Terminal Disclaimer

☐ Petition to Commissioner

☐ Status Inquiry

☐ Other ____

OIPE JC174 NOV 06 2003 PATENT & TRADEMARK OFFICE

OIPE DEC 23 2004 PATENT & TRADEMARK OFFICE

OIPE DEC 23 2004 PATENT & TRADEMARK OFFICE

Check for $		☒ Charge Deposit Acct. 500417$	212.00	Atty Init.	MEF/ RMF	Tkpr. #	3328	Secy. or PL:	AM. Ziegler

CMS Descrip.: (3) 212.00

THE PATENT AND TRADEMARK OFFICE DATE STAMPED HEREON IS ACKNOWLEDGEMENT THAT THE ITEMS, CHECKED ABOVE, WERE RECEIVED BY THE PTO ON THE DATE STAMPED.

Docket No.: 60188-415

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Takenobu KISHIDA, et al.

Serial No.: 10/036,388

Filed: January 07, 2002

Customer Number: 20277

Confirmation Number: 3663

Group Art Unit: 2814

Examiner: Phat X. CAO

For: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

Mail Stop Fee Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Transmitted herewith is an Amendment in the above-identified application.

☐ No additional fee is required.
☐ Applicant is entitled to small entity status under 37 CFR 1.27
☐ Also attached:

The fee has been calculated as shown below:

	NO. OF CLAIMS	HIGHEST PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	27	20	7	$18.00 =	$126.00
Independent Claims	4	3	1	$86.00 =	$86.00
		Multiple claims newly presented			$0.00
		Fee for extension of time			$0.00
					$0.00
				Total of Above Calculations	$212.00

☒ Please charge my Deposit Account No. 500417 in the amount of $212.00. An additional copy of this transmittal sheet is submitted herewith.

☒ The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 500417, including any filing fees under 37 CFR 1.16 for presentation of extra claims and any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

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Date: November 6, 2003

Docket No.: 60188-415

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer No.: 20277
Takenobu KISHIDA et al.	:	Confirmation No.: 3663
Serial No.: 10/036,388	:	Group Art Unit: 2814
Filed: January 7, 2002	:	Examiner: Phat X. CAO

For: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

AMENDMENT

Mail Stop Fee Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated August 19, 2003, having a three-month shortened statutory period for response set to expire on November 19, 2003, reconsideration of the above-identified application is respectfully requested in view of the following amendment and remarks.

IN THE TITLE

Please replace the existing title with the following new title:

--SEMICONDUCTOR DEVICE INCLUDING A LAYER HAVING A β-CRYSTAL STRUCTURE--

AMENDMENT TO THE CLAIMS

19. (Previously presented) A semiconductor device comprising:

an insulating film formed on a semiconductor substrate;

a lower interconnect formed in the insulating film;

a via hole formed on the lower interconnect and in the insulating film;

an interconnect groove formed in an upper region of the via hole and in the insulating film;

a plug composed of a conducting film buried in the via hole;

an upper interconnect buried in the interconnect groove; and

a barrier layer formed between the insulating film and the plug, the insulating film and the upper interconnect, and the plug and the lower interconnect,

wherein the conducting film comprises copper, aluminum or silver,

wherein the barrier layer is composed of a laminated film including a lower first barrier layer and an upper second barrier layer, and

wherein the first barrier layer is made from a tantalum nitride film, and the second barrier layer is made from a tantalum film having a β-crystal structure.

20. (Previously presented) The semiconductor device of Claim 19, wherein the conducting film is a copper film.

21. (Previously presented) The semiconductor device of Claim 20, wherein the copper film is oriented to the (111) plane.

22. (Previously presented) The semiconductor device of Claim 19, wherein a value of (a number of nitrogen atoms)/(a number of tantalum atoms) of the tantalum nitride film is 0.4 or less.

23. (Previously presented) The semiconductor device of Claim 19, wherein the insulating film includes a fluorine component.

24. (Previously presented) The semiconductor device of Claim 19, wherein the second barrier layer is deposited on the first barrier layer.

25. (Previously presented) A semiconductor device comprising:

an insulating film formed on a semiconductor substrate;

a lower interconnect formed in the insulating film;

a first interlayer insulating film formed on the lower interconnect and the insulating film;

a via hole formed on the lower interconnect and in the first interlayer insulating film;

a second interlayer insulating film formed on the first interlayer insulating film;

an interconnect groove formed in an upper region of the via hole and in the second interlayer insulating film;

a barrier layer formed respectively on a bottom and walls of the via hole and the interconnect groove; and

a plug and an upper interconnect composed of a conducting film formed on the barrier layer provided in the via hole and the interconnect groove,

wherein the conducting film comprises copper, aluminum or silver,

wherein the barrier layer is composed of a laminated film including a lower first barrier layer and an upper second barrier layer, and

wherein the first barrier layer is made from a tantalum nitride film, and the second barrier layer is made from a tantalum film having a β-crystal structure.

26. (Previously presented) The semiconductor device of Claim 25, wherein the conducting film is a copper film.

27. (Previously presented) The semiconductor device of Claim 26, wherein the copper film is oriented to the (111) plane.

28. (Previously presented) The semiconductor device of Claim 25, wherein a value of (a number of nitrogen atoms)/(a number of tantalum atoms) of the tantalum nitride film is 0.4 or less.

29. (Previously presented) The semiconductor device of Claim 25, wherein the first interlayer insulating film or the second interlayer insulating film includes a fluorine component.

30. (Previously presented) The semiconductor device of Claim 19, wherein the second barrier layer is deposited on the first barrier layer.

31-36. (Canceled)

37. (New) A semiconductor device, comprising:

an insulating film including a recess formed therein,

a conducting film formed in the recess; and

a laminated film formed between the insulating film and the conducting film,

wherein the conducting film comprises copper, aluminum or silver,

wherein the laminated film includes a lower first barrier layer and an upper second barrier layer, and

wherein the first barrier layer is made from a tantalum nitride film, and the second barrier layer is made from a tantalum film having a β-crystal structure.

38. (New) The semiconductor device of claim 37, wherein the recess comprises a via hole and an interconnect groove.

39. (New) The semiconductor device of claim 38, further comprising:

a plug formed in the via hole; and

an interconnect formed in the interconnect groove.

40. (New) The semiconductor device of Claim 37, wherein the conducting film includes a copper film.

41. (New) The semiconductor device of Claim 40, wherein the copper film is oriented to the (111) plane.

42. (New) The semiconductor device of Claim 37, wherein a value of (a number of nitrogen atoms)/(a number of tantalum atoms) of the tantalum nitride film is 0.4 or less.

43. (New) The semiconductor device of Claim 37, wherein the insulating film includes a fluorine component.

44. (New) A semiconductor device, comprising:

an insulating film;

a conducting film formed on the insulating film; and

a barrier layer formed between the insulating film and the conducting film,

wherein the barrier layer is made from a tantalum film having a β-crystal structure, and

wherein said barrier layer and conducting film are sequentially deposited so that at least a portion of the barrier layer directly contacts the conducting film after which an annealing step is conducted, and

wherein after the annealing step, said at least a portion of the barrier layer directly contacts the conducting film.

45. (New) The semiconductor device of claim 44, wherein the conducting film comprises copper, aluminum or silver.

46. (New) The semiconductor device of claim 44, wherein the insulating film includes a recess and said conducting film being formed in said recess.

47. (New) The semiconductor device of claim 46, wherein the recess comprises a via hole and an interconnect groove.

48. (New) The semiconductor device of claim 47, further comprising:

a plug formed in the via hole; and

an interconnect formed in the interconnect groove.

49. (New) The semiconductor device of Claim 44, wherein the conducting film includes a copper film.

50. (New) The semiconductor device of Claim 49, wherein the copper film is oriented to the (111) plane.

51. (New) The semiconductor device of Claim 44, wherein the insulating film includes a fluorine component.

REMARKS

Claims 19-24 stand rejected under 35 U.S.C. § 103 as being unpatentable over Cabral, Jr. et al. '440 ("Cabral") in view of Kwon et al. ("Kwon"), and claims 25-30 stand rejected under 35 U.S.C. § 103 as being unpatentable over Cabral in view of Kwon and Grill et al. '747 (Grill et al. relied on only for dividing the interlayer insulating film). Claims 19 and 25 are independent. These rejections are respectfully traversed for the following reasons.

Claims 19 and 25 each embody a first barrier layer that is made from a tantalum nitride film and a second barrier layer that is made from a tantalum film having a β-crystal structure. It is respectfully submitted that neither Cabral nor Kwon, alone or in combination, disclose or suggest the ***combination*** of a TaN/Ta(β-crystal) laminated layer. The Examiner relies on Cabral for disclosing a laminated TaN/Ta(α-crystal) layer and relies on the single Ta(β-crystal) layer taught by Kwon to modify Cabral in an attempt to reach the claimed invention.

However, Kwon discloses only a Ta(β-crystal) formed on a silicon oxide insulating layer under conditions whereby the β-crystal structure can be formed. Indeed, this is merely cumulative to the prior art described at col. 1, lines 49-52 of Cabral regarding a single beta Ta layer formed on an insulator such as silicon oxide, whereas Cabral is specifically directed to forming an α-crystal Ta layer ***so as to avoid*** the high-resistivity β-crystal Ta layer. To accomplish this, Cabral expressly discloses a ***hexagonal*** phase TaN as the underlayer so that a Ta layer formed thereon can ***only*** have an α-crystal structure (***see* col. 6, lines 14-22 of Cabral**). Neither Cabral nor Kwon disclose or suggest the combination of a Ta film having a β-crystal structure on a TaN film, let alone

enable such an arrangement. As mentioned above, Cabral's underlayer is specifically configured to allow only an α-crystal to be formed thereon and to prevent formation of a β-crystal structure.

The Examiner is directed to MPEP § 2143.03 under the section entitled "All Claim Limitations Must Be Taught or Suggested", which sets forth the applicable standard:

> To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, the pending rejection does not "establish *prima facie* obviousness of [the] claimed invention" as recited in claims 19 and 25 because the proposed combination fails the "all the claim limitations" standard required under § 103.

Moreover, any attempt to modify Cabral to utilized a laminate including Ta(β-crystal) would render Cabral unsatisfactory for its expressly stated purpose of a reduced resistivity by NOT using a β-crystal structure. The Examiner is directed to MPEP § 2143.01 under the sub-title "The Proposed Modification Cannot Render the Prior Art Unsatisfactory for its Intended Purpose", which sets forth:

> If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. (citing *In re Gordon*, 221 USPQ 1125 (Fed. Cir. 1984)).

Furthermore, the asserted motivation of improving adhesion is based on the assumption that a Ta(β-crystal) is being used in the first place. That is, Kwon does not suggest using Ta(β-crystal) to improve adhesion. Rather, Kwon suggests forming an interfacial layer to improve the adhesion ***specifically of a Ta(β-crystal)***. In other words, the improved adhesion of Kwon is NOT derived from using a Ta(β-crystal) layer rather

than a Ta (α-crystal) layer, but instead, the improved adhesion is derived from forming an interfacial layer when already using a poorly adhered Ta(β-crystal) layer. Indeed, Cabral appears to suggest at col. 1, lines 49-50 that Ta(β-crystal) adheres poorly and Kwon merely discloses how to improve adhesion specifically in a Ta(β -crystal) layer by forming an interfacial layer. Whereas, Cabral uses a α-crystal Ta layer and teaches away from a Ta(β-crystal) layer so as to have no need for a Ta(β-crystal) layer, let alone improved adhesion. In this regard, Cabral teaches away from the claimed invention. The Examiner is directed to MPEP § 2141.02 under the section entitled "Prior Art Must Be Considered in its Entirety, Including Disclosures that Teach Away from the Claims", which sets forth the applicable standard:

> A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. (citing *Gore v. Garlock*, 220 USPQ 303 (Fed. Cir. 1983)).

Accordingly, the teachings of Kwon are not applicable to Cabral because to begin with, Cabral does not use a β -crystal Ta layer whose adhesive property needs to be improved by forming an interfacial layer. It is therefore respectfully submitted that there is no motivation to replace the Ta(α-crystal) layer of Cabral with the Ta(β-crystal) of Kwon for the asserted motivation of improving adhesion because Cabral already has a better adhesive property using the Ta(α-crystal) layer.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claims 19 and 25 are patentable for the reasons set forth above, it is respectfully

submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

For example, with respect to claims 22 and 28, the Examiner apparently relies on col. 2, lines 49-54 of Cabral as allegedly disclosing "wherein a value of (a number of nitrogen atoms)/(a number of tantalum atoms) of the tantalum nitride film is 0.4 or less." However, Cabral discloses only that the N/TaN ratio ranges from 30-60%. That is, the nitrogen content relative to TaN ranges from 0.3-0.6, whereby the corresponding Ta content relative to TaN is 0.7-0.4, respectively. Accordingly, the N/Ta ratio ranges from 0.3/0.7 to 0.6/0.4, that is, 0.43-1.5. In contrast, claims 22 and 28 embody a N/Ta ratio of 0.4 or less, which ratio can help enable forming the Ta(β-crystal) on the TaN film. As mentioned above, Cabral does not desire a β-crystal structure and therefore expressly teaches away from a N/Ta ratio that can enable formation of a β-crystal structure.

Based on all the foregoing, it is submitted that claims 19-30 are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejection of claims 19-30 under 35 U.S.C. § 103 be withdrawn.

New claims 37-43 are submitted to be patentable for reasons similar to those discussed above.

New claims 44-51 are submitted to be patentable over the cited prior art. In order to clarify the distinction between claim 44 and the cited prior art, a personal interview was conducted with Examiner Cao. Applicants and Applicants' representative would like to thank Examiner Cao for his courtesy in conducting the interview and for his assistance in resolving issues.

As a preliminary matter, it is respectfully submitted that the product-by-process limitation recited in claim 44 must be given patentable weight because it implies the structure of the invention by imparting distinctive structural characteristics to the final product. The Examiner is directed to MPEP § 2113, which sets forth the applicable standard:

> The structure implied by the process steps should be considered when assessing the patentability of product-by-process claims over the prior art, especially ... where the manufacturing process steps would be expected to impart distinctive structural characteristics to the final product. (citing *In re Garnero*, 162 USPQ 221 (CCPA 1979)).

In the instant case, the claimed depositing and annealing process impart a distinctive structural characteristic in that an interfacial layer between the barrier layer and conducting film is not formed so that the ***final*** product, to be used in actual devices, has at least a portion of the barrier layer which directly contacts the conducting film. In contrast, Kwon expressly discloses annealing at a sufficient temperature to form the interfacial layer as part of the final product which prevents the copper and Ta films to directly contact each other. Indeed, as set forth on lines 4-5 of the Abstract, Kwon states that "Cu reacts readily at 400°C with Ta to form a thin interfacial amorphous interfacial layer that promotes the adhesion of Cu to Ta." That is, Kwon expressly controls the parameters of the annealing process to ensure formation of the interfacial layer for the final product as a means to improve the adhesion between the Cu/Ta layer, so as to prevent contact between the Cu and Ta layers in the final product.

In contrast, claim 44 embodies a process by which an annealing step is conducted which does not form an interfacial layer that prevents the barrier layer and conducting film from directly contacting each other after the anneal (e.g., 150°C; *see, e.g.*, page 13,

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Michael E. Fogarty
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Date: November 6, 2003